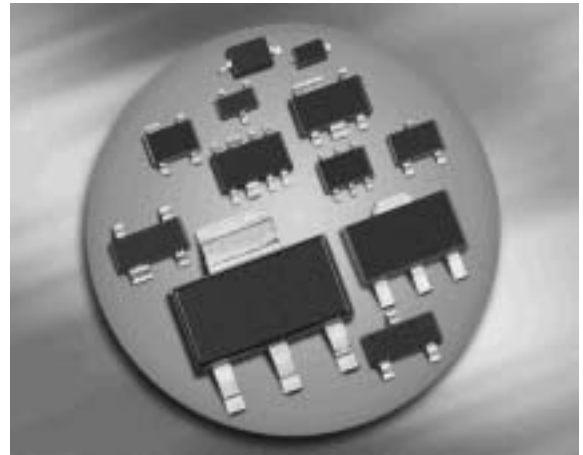
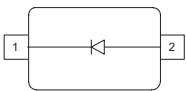


Silicon Tuning Diodes

- High Q hyperabrupt tuning diode
- Designed for low tuning voltage operation
- For VCO's in mobile communications equipment
- Pb-free (RoHS compliant) package¹⁾
- Qualified according AEC Q101



BBY52-02L
BBY52-02W



Type	Package	Configuration	L_S (nH)	Marking
BBY52-02L	TSLP-2-1	single, leadless	0.4	K
BBY52-02W	SCD80	single	0.6	KK

Maximum Ratings at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Diode reverse voltage	V_R	7	V
Forward current	I_F	20	mA
Operating temperature range	T_{op}	-55 ... 150	°C
Storage temperature	T_{stg}	-55 ... 150	

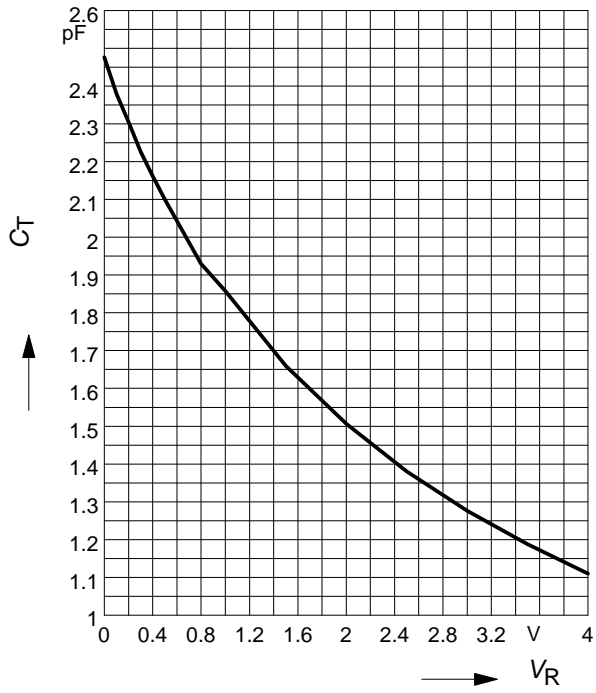
¹⁾Pb-containing package may be available upon special request

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Reverse current	I_R				nA
$V_R = 6\text{ V}$		-	-	10	
$V_R = 6\text{ V}, T_A = 85^\circ\text{C}$		-	-	200	
AC Characteristics					
Diode capacitance	C_T				pF
$V_R = 1\text{ V}, f = 1\text{ MHz}$		1.4	1.85	2.2	
$V_R = 2\text{ V}, f = 1\text{ MHz}$		0.95	1.5	2	
$V_R = 3\text{ V}, f = 1\text{ MHz}$		0.9	1.35	1.75	
$V_R = 4\text{ V}, f = 1\text{ MHz}$		0.85	1.15	1.45	
Capacitance ratio	C_{T1}/C_{T4}	1.1	1.6	2.1	
$V_R = 1\text{ V}, V_R = 4\text{ V}, f = 1\text{ MHz}$					
Series resistance	r_S	-	0.9	1.7	Ω
$V_R = 1\text{ V}, f = 1\text{ GHz}$					

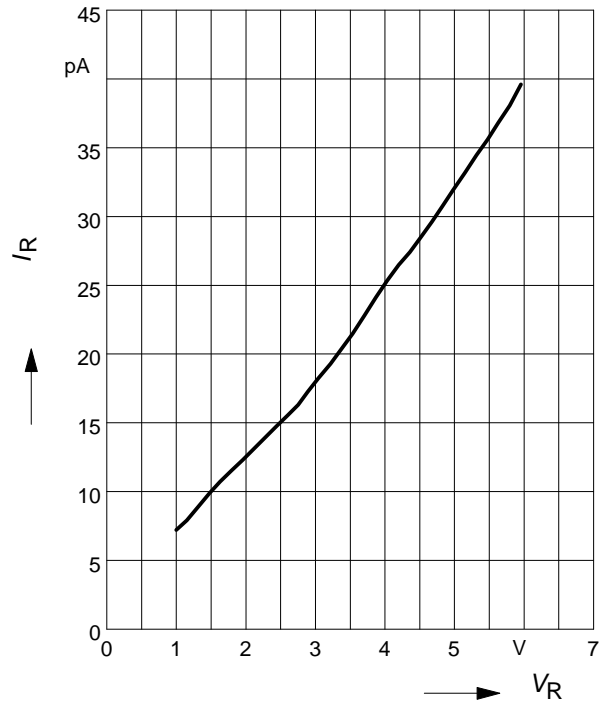
Diode capacitance $C_T = f(V_R)$

$f = 1\text{MHz}$

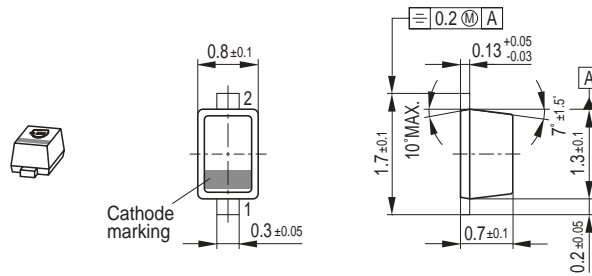


Reverse current $I_R = f(V_R)$

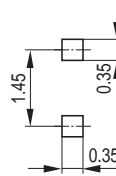
$T_A = 25^\circ\text{C}$



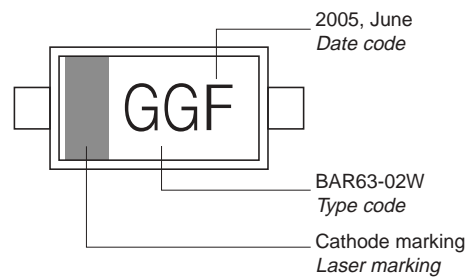
Package Outline



Foot Print

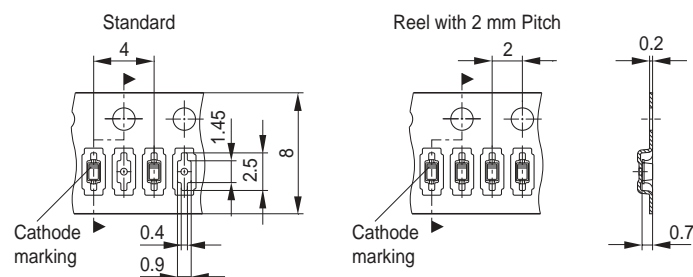


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
 Reel ø180 mm = 8.000 Pieces/Reel (2 mm Pitch)
 Reel ø330 mm = 10.000 Pieces/Reel

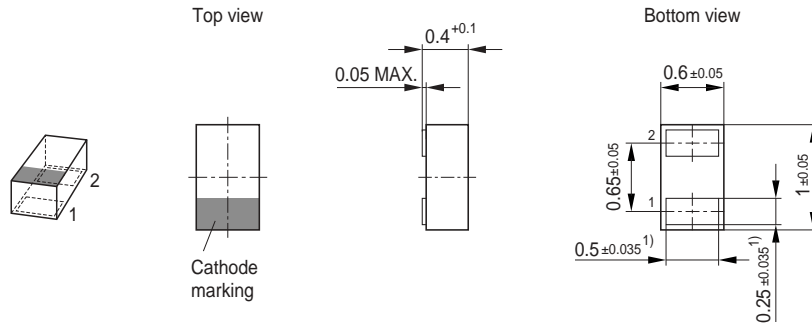


Date Code marking for discrete packages with one digit (SCD80, SC79, SC75¹⁾) CES-Code

Month	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
01	a	p	A	P	a	p	A	P	a	p	A	P
02	b	q	B	Q	b	q	B	Q	b	q	B	Q
03	c	r	C	R	c	r	C	R	c	r	C	R
04	d	s	D	S	d	s	D	S	d	s	D	S
05	e	t	E	T	e	t	E	T	e	t	E	T
06	f	u	F	U	f	u	F	U	f	u	F	U
07	g	v	G	V	g	v	G	V	g	v	G	V
08	h	x	H	X	h	x	H	X	h	x	H	X
09	j	y	J	Y	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5	n	3	N	5

1) New Marking Layout for SC75, implemented at October 2005.

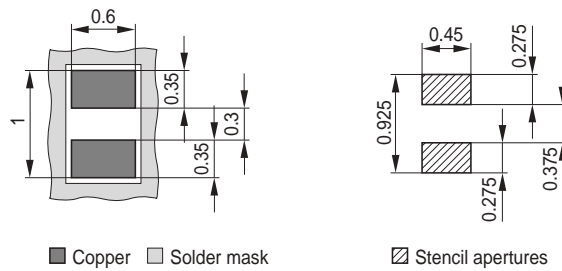
Package Outline



1) Dimension applies to plated terminal

Foot Print

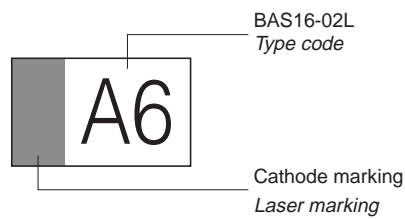
For board assembly information please refer to Infineon website "Packages"



■ Copper □ Solder mask

▨ Stencil apertures

Marking Layout (Example)

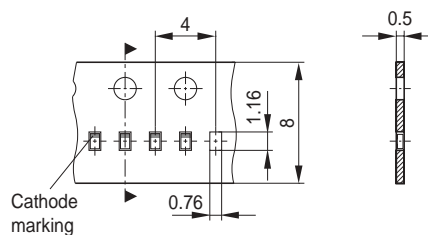


BAS16-02L
Type code

Cathode marking
Laser marking

Standard Packing

Reel \varnothing 180 mm = 15.000 Pieces/Reel
Reel \varnothing 330 mm = 50.000 Pieces/Reel (optional)



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